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ESD PROTECTION SYSTEM FOR HIGH FREQUENCY APPLICATIONS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to electrostatic discharge (ESD) protection circuits, and more particularly to ESD circuits for multiple power supplies in radio frequency (RF) applications.

2 Description of the Related Art

Integrated circuits, especially silicon integrated circuits (IC), are susceptible to damage caused by electrostatic discharge from environmental sources. Such sources of relative charge are human beings handling the wafer, die, or packaged IC, improperly grounded test and assembly equipment, and the device itself, which may accumulate charge during storage and transport. To avoid these post-fabrication yield losses, each IC must be designed to withstand the likely types of environmental electrostatic discharge it may face. The basic models used are the Human Body Model (HBM) as per FIG. 1, Machine Model (MM), and the Charged Device Model (CDM).

In FIG. 1 a schematic for a Human Body Model (HBM) type ESD discharge tester is shown to the left of the dotted line. The 100pF capacitor 11 and the 1.5kOhm resistor 12 are essential to the model. The inductance 13 and other capacitances 14

and 15 are parasitic elements of the tester. The Device Under Test (DUT) 16 is shown to the right of the dotted line. In evaluation of the proposed ESD protection system, the inventors used the HBM in all of their testing.

Special devices are placed in the layout of the IC to steer the discharge current away from the functional IC circuitry. The scheme we have used in our implementation is based upon the prior art dual-diode and shunt scheme 200 shown in FIG. 2. The diodes 204, 205 connecting the I/O pads 202 to the power supply rails 206, 207 (and the Vss to Vdd diode 208) along with the power shunt 210, which connects the power supply rails in the case of a positively ramped voltage from Vdd to Vss, provide a low impedance path for current flow between any two pins when the IC is powered down. For example, a positive spike from an I/O pad to Vss will cause current to run through a P+/N-well diode 204 and then down through the power shunt circuit 210. The I/O circuits and core 214 receive their input directly from the I/O pads. The resistances 212 shown in the power supply rails are parasitic resistances that lead to voltage drops during the current pulse.

For the system to work properly, each current steering element (the diodes and the shunt) must drop as little voltage for as high a current as possible. Moreover, the parasitic metal resistances must be accounted for and understood. Therefore, the shunts and diodes must be well designed to be as efficient as possible.

RF circuits have an additional constraint that the diodes 204, 205 on the input pads 202 must present very little capacitive loading to the signal compared with the amount that lower frequency parts can tolerate. In addition, this capacitance should preferably be bias-independent. The low-loading requirement dictates that the diodes must be scaled down, thus raising the voltage drop for a given ESD current. To compensate for this, the power shunt circuit must be designed to be very robust to allow for the greater drop from the I/O pad diodes 204, 205.

The diode-coupling and shunt scheme proposed by the inventors contrasts with those by Stackhouse et al. (U.S. Patent 5,740,000), Worley et al. (U.S. Patent 5,654,862), Maloney (U.S. Patent 5,530,612), and Gens et al. (U.S. Patent 5,515,225). The difference is that all of these use a single main shunt between two power supply nodes and couple other power supplies (including the Vdd supplies) via diodes or bridge circuits.

The clamp of the power shunt circuit differs from the one used by Stackhouse, et al. (U.S. Patent 5,740,000) in the implementation of the RC timer. Prior art power shunt circuits are also shown by Miller et al. (U.S. Patent 5,946,177) and Shay (U.S. Patent 5,508,649) but differ in the implementation.

The proposed three-inversion RC-timed shunt for the power shunt circuit is superior to the one used by Ker (U.S. Patent 5,744,842) and Strauss (U.S. Patent

5,559,659) because of the advantage which PMOS devices provide and which will be shown in the body of the proposed invention.

Other U.S. Patents not already mentioned, but relating to the present invention, are:

U.S. Patent 6,091,593 (Lin) discloses an RC timed ring-oscillator charge pump for inducing turn-on in MOS or bipolar protection devices.

U.S. Patent 6,072,682 (Ravanelli et al.) describes an all NMOS RC-triggered source-follower shunt.

U.S. Patent 6,014,298 (Yu) discloses an RC timed switch to be placed in series between power Vcc and circuit to be protected. The switch turns off when an ESD is detected to prevent discharge going through the core circuit.

U.S. Patent 5,986,861 (Pontarollo) presents a simple clamp, with a PMOS final transistor and NMOS inverter triggered by RC.

U.S. Patent 5,907,464 (Maloney et al.) describes a shunt circuit with a PMOS final driver and timed by a PMOS resistor/generic capacitor time constant.

U.S. Patent 5,745,323 (English et al.) teaches an input line protection circuit which uses RC-timed PMOS and NMOS transistors to discharge ESD current to the Vdd and Vss power rails.

U.S. Patent 5,287,241 (Puar) discloses a PMOS final driver triggered and timed by a PMOS resistor/NMOS capacitor RC.

U.S. Patent 5,255,146 (Miller) describes an NMOS final driver with three RC timers, feedback loop, and NAND gate triggering to detect the rise time of the ESD, to insure that the ESD is longer than a typical noise pulse.

SUMMARY OF THE INVENTION

It is an object of the present invention to steer ESD currents away from the functional IC circuitry and thus protect this circuitry when an ESD is applied between any two pads of the IC in any direction, in particular with respect to RF IC circuitry.

It is another object of the present invention to provide this protection from ESD currents to circuits which utilize multiple power supply rails for both the more positive, Vdd, and the more negative, Vss, power supply rail.

It is yet another object of the present invention to provide complete isolation of the Vdd busses so that noise on one Vdd bus does not directly couple to another Vdd bus.

It is still another object of the present invention to provide this isolation with low capacitive loading for radio frequency (RF) systems.

It is a further object of the present invention to allow operation of the various Vdd busses at any supply voltage required for circuit operation.

It is yet a further object of the present invention to provide operation in which the various Vss busses may differ in potential by up to a single diode drop.

It is still a further object of the present invention to provide operation in which the various Vss busses are at the same potential and are joined together through the resistive substrate.

These and many other objects have been achieved by:

connecting together Vss busses by a pair of complementary polarity diodes made typically with P+/N-well diodes in an N /P-substrate process;

paying special attention to the I/O diodes of high frequency I/O pads, such that no resistance is in the signal path, and that the capacitance per diode is kept to less than 200 femto-Farads (200×10^{-15} F);

special diode layout to insure that the highest current capacity per femto-Farad of loading capacitance is achieved;

insuring that the worst case ESD event will flow at most between two I/O pads and one power shunt;

insuring that the power shunt circuit clamps are at a very low voltage during an ESD event;

providing each pair of power rails its own shunt circuit thus placing each shunt in physical proximity to the I/O pad it must protect; and

providing an I/O diode layout with the largest perimeter/area ratio possible.

These and many other objects and advantages of the present invention will be readily apparent to one skilled in the art to which the invention pertains from a perusal of the claims, the appended drawings, and the following detailed description of the preferred embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of the Human Body Model (HBM) type ESD discharge tester.

FIG. 2 is a circuit diagram of a dual-diode and power rails shunt for a single pair of power rails and multiple I/O pads of the prior art.

FIG. 3 is a high level circuit diagram of a general RF ESD protection scheme of the present invention.

FIG. 4 is a circuit diagram of a simple power shunt circuit according to a first preferred embodiment of the present invention.

FIG. 5 is a circuit diagram of a more complex power shunt circuit having a lower clamping voltage than the circuit of FIG. 4 according to a second preferred embodiment of the present invention.

FIG. 6 is a top view of the layout used for an I/O diode of the present invention.

FIG. 7 is a top view of a plurality of I/O diodes of FIG. 6, scaled up by arraying the basic layout.

FIG. 8 is a graph illustrating the I/O diode pair capacitance vs. pad bias.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The general layout of the radio frequency (RF) electrostatic discharge (ESD) protection invention 300 is shown in FIG. 3. Multiple I/O pads for each power supply rail pair are assumed, although only one is shown for each power supply rail pair in FIG. 3. The same numerals in FIG. 2 and FIG. 3 designate the same component.

In this invention, multiple power supply rail pairs are connected together through the various Vss busses only, which are connected together by a pair of complementary polarity diodes 340, also called Vss coupling diodes. The Vdd busses 316, 326, 336 remain completely isolated so that noise on one Vdd bus does not directly couple to

another Vdd bus. This is important for RF systems in which various circuit blocks must be well isolated from one another. Also notice in this system that the various Vdd busses 316, 326, 336 may operate at any supply voltages required for circuit operation.

This invention is applicable for systems in which the various Vss bus voltages do not differ by more than a single diode drop. In most cases, all Vss busses will be at the same potential and will often be connected together through the resistive substrate, and they may be isolated solely to further limit supply noise cross talk. In the case that the various Vss busses are shorted together by metal, i.e. there is just a single common Vss node, the system works just as well for ESD (even better, actually) while allowing the Vdd busses to remain separate. Inspection of the system reveals that an ESD current pulse between any two I/O pads 312, 322, 332 in any direction will result in at most a three diode and one power shunt voltage drop, plus parasitic voltage drops due to resistance in the routing (not shown). Similarly, an ESD event between an I/O pad and Vdd or Vss equals a two diode and one power shunt voltage drop. While FIG. 3 illustrates three separate systems 310, 320, and 330 it is well understood that this number can vary to suit the particular design.

The Vss coupling diodes 340 are typically made with P+/N-well diodes in an N-well/P-substrate process. N+/P-substrate diodes may be used if the Vss busses to be connected are tied to the substrate. In this case, pseudo-isolation of the various Vss

busses simply requires that any P+ substrate taps remain far enough apart to provide resistive isolation through the substrate.

The diodes on any high frequency I/O pads, such as the RF signal pads, require special attention. In addition to the requirement that no resistance may be in the signal path, capacitance must be managed and typically kept very low, typically less than 200fF (fF=femto Farad=10^{-15} Farad) per diode to prevent signal loss through the ESD diodes during circuit operation. Special diode layout must be used to insure that the highest current carrying capacity possible per femto-Farad of loading capacitance is achieved. Nevertheless, scaling the capacitance down inevitably causes current carrying capability to drop, which implies a larger voltage drop across the diode for a given ESD current. Because the worst case ESD event will flow between two I/O pads and the power shunt 210, the power shunt must be designed to clamp at a very low voltage during an ESD event.

A further aspect of the system is that each pair of power supply rails 316/317, 326/327, 336/337 needs its own power shunt circuit 210 to conduct current for a positive pulse from Vdd to Vss. The drawback of this is that it will of course consume more silicon area than an optimal ESD system for non-Vdd-isolated systems. But the advantage of this separated shunt system is that it places each shunt in physical proximity to the I/O pads (e.g., 312, 322, 332) it must protect. Because most circuit components are connected to a single pair of power supply rails only, the voltage drop

of consequence is the total across the single pair of power supply rails at issue. Thus, the consequences of the ESD pulse are divided and conquered by this system. Special attention needs to be paid only to the interface devices where power bus resistances will have the largest impact.

We now describe the circuit of FIG. 3 in greater detail. The general RF ESD protection circuit 300 comprises three protection circuits 310, 320, and 330. The number of protection circuits shown is for illustration purposes only and could be more or less than three. Each power supply rail is connected to a pair of power pads Vdd1/Vss1 (311/319), Vdd2/Vss2 (321/329), Vdd3/Vss3 (331/339). Coupled between the power rails of each protection circuit are first and second I/O diodes 204 and 205. I/O pads 312, 322, 332, the inputs to the protection circuits, are coupled to the junction of these I/O diodes. In one preferred embodiment of the present invention the power rails Vss1, Vss2, and Vss3 are connected directly to each other. In a second preferred embodiment these power rails are coupled together via complementary polarity diodes 340. In the example of FIG. 3, three sets of these complementary polarity diodes are required. The number of complementary polarity diodes is determined by the combinatorial function, e.g. four protection circuits require 6 sets of complementary polarity diodes.

Power Shunt Circuit

The circuits of FIG. 4 and FIG. 5 are transient-type, designed to turn on when the voltage ramp on Vdd is faster than an RC time-constant and greater than PMOS Vt. When no power is applied to the circuit (as is the case when most ESD damage occurs), all nodes are at the same potential. From FIG. 4, we see that when a positive voltage spike occurs at Vdd, node A is held low by PMOS capacitor M11. This voltage difference turns on device M2 which allows node D to follow Vdd. Thus, M1 is diode-connected to Vdd and clamps Vdd until node A charges through devices, M8-M10. The CMOS inverter driver 430, formed by devices M2 and M3, has a trip point skewed high to speed the turn-on of device M1. The same numerals in FIG. 4 and FIG. 5 designate the same component.

We now describe the circuit of FIG. 4 in greater detail. Power shunt circuit 210 comprises RC timer 410 and CMOS inverter driver 430. The RC timer is coupled between Vdd, the first power supply rail, and Vss, the second power supply rail. The RC timer comprises PMOS transistors M8, M9, and M10 (the first, second and third PMOS transistor) all connected in series, where the source of M8 is coupled to Vdd. The gates of M8, M9, and M10 are coupled to Vss. The drain of M10 is coupled to node A and to the gate of PMOS transistor M11 (the fourth PMOS transistor). The source and drain of M11 are coupled to Vss. The gates of PMOS transistors M2 (the fifth PMOS transistor) and M3 (the first NMOS transistor) are coupled to node A. The junction of M2 and M3 forms node D which is coupled to the gate of output NMOS transistor M1 (the second NMOS transistor). The width ratio of M2 to M3 is typically

4:1. The output transistor M1 has a typical width/length dimension of 2000/0.35 micron. The numbers next to each transistor give the preferred width and length of the transistor. However, these dimensions can vary to suit the specific design.

FIG. 5 shows the enhanced version of this type of clamp. It is designed to clamp Vdd to a lower voltage through the much larger M1 transistor. The width of transistor M1 is now reduced to typically 6000μm (μm=micron). The clamp of FIG. 5 also has two further inverter stages 510, 520 (devices M6, M7 and M4, M5, respectively) and a further capacitor M12 to enhance the turn-on speed. The RC timer 410 is identical to that in FIG. 4. Device M2 of CMOS inverter driver 430 is made larger to provide necessary drive to the larger M1 device during turn-on. Device M12 holds node C low when a spike occurs at Vdd so that the bootstrap effect of the drain-to-gate capacitance of M2 is diminished. Thus, capacitive voltage division between M2 and M12 initiates turn-on. The inverter 520 formed by M4 and M5 is also skewed to preferentially keep node C low during an ESD event. The inverter 510 formed by M6 and M7, however, has a normal mid-swing trip-point so that during normal operation, noise at Vdd will not turn the shunt on for longer than the RC time-constant formed by resistance M4 and the capacitance at node C.

We now describe the circuit of FIG. 5 in greater detail. In the second preferred embodiment of the present invention the power shunt circuit 210 of FIG. 4 is enhanced to clamp Vdd to a lower voltage as already stated earlier. First inverter 510 is coupled

between Vdd (first power supply rail) and Vss (second power supply rail) and its input connects to node A. Its output is node B which is also the junction of M6 and M7. Second inverter 520 is similarly coupled between Vdd and Vss and its input connects to node B. Its output is node C which is also the junction of M4 and M5. A sixth PMOS transistor M12 is wired as a capacitor by coupling the drain and source to Vss. The gate of M12 is connected to node C. The gates of PMOS transistors M2 (the fifth PMOS transistor) and M3 (the first NMOS transistor) are also coupled to node C. Note that the width of M2 in FIG. 5 was increased to 800µm from 400µm in the embodiment of FIG. 4.

Referring to both FIG. 4 and FIG. 5, the RC timer 410 itself is made exclusively from PMOS devices M8, M9, M10, and M11. Devices M8-M10 provide a large resistance in a small area. PMOS devices M11 and M12 are used rather than NMOS devices because they are operated in the accumulation region and provide a large capacitance through the full range of operation. An NMOS device used in a similar position presents a lower capacitance from 0V to Vt and is thus more easily bootstrapped up to Vt.

I/O Diodes

The diodes, such as 204, 205 of FIG. 3, used on the I/O pads 312, 322, 332 must provide the highest current carrying capacity per unit of capacitance possible. The preferred embodiment of the diode layout is shown in FIG. 6.

Still referring to FIG. 6, the layout 60 shown is of an N+/P-substrate diode 205 (second I/O diode) for connection between I/O pad (e.g. 312) and Vss. The P+/N-well diode 204 (first I/O diode) is identical but having complementary diffusions. The central square 62 is an N+ diffusion, which forms the diode junction with the substrate. The surrounding ring 64, of width S, is the p-base (or n-base for complimentary diodes). The width S between the diffusions 62 and 66 is set to minimum to provide lowest resistance. The N+ diffusion is square to provide the largest Perimeter/Area ratio, which is shown to provide the best current/capacitance ratio. The length W of each side of the square is set by the number of contacts 68 needed to pass the target current. Four contacts 68 are shown by way of illustration. The actual number used depends on the application. This diode layout is different than the standard finger-type layout that uses long, rectangular, minimum width diffusions rather than squares. While a square configuration of layout 60 is the preferred embodiment for the above stated reasons, other shapes such as, but not limited to, a rectangular configuration are possible. FIG. 7 is a layout which shows how ESD protection and capacitance can be scaled by arraying the basic layout of FIG. 6. FIG. 7 depicts a 4 by 4 array by way of example. It is obvious to those skilled in the art that any other dimensioned square or rectangular array is equally feasible.

The first I/O diode 204 is coupled between I/O pad (e.g. 312) and Vdd such that the anode connects to the I/O pad and the cathode to Vdd. The anode and the cathode correspond to the P+ diffusion and the N-well, respectively. The P+ diffusion relates to the central square 62 of FIG. 6, and the N-well base of width S relates to the surrounding ring 64. Because both diodes 204 and 205 direct current in the same direction, the anode of the second I/O diode 205 connects to Vss and the cathode to the I/O pad. The cathode and anode of I/O diode 205 correspond to the N+ diffusion and P-substrate, respectively.

Another advantage of the I/O dual-diode invention is that the capacitance at the input node such as 312 is relatively bias independent. FIG. 8 shows this relationship. Curve 1 shows the capacitance vs. I/O pad bias for the P+/N-well diode, e.g. 204, Curve 2 shows the capacitance vs. I/O pad bias for the N+/P-substrate diode, e.g. 205, and Curve 3, the sum of the Curve 1 and 2, graphs the response of the diode pair. This is a characteristic of the dual-diode invention itself, rather than the square layout per se. Other layout geometry of the dual-diodes would also exhibit a similar characteristic.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is: